

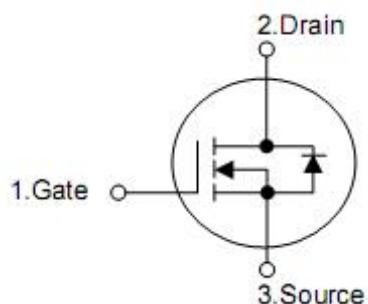
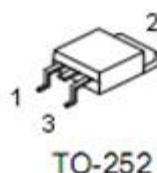
1. Features

- RDS(on)=3.2mΩ@ VGS=10V
- Uses CRM(CQ) advanced Trench MOS technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent QgxR_{DS(on)} product(FOM)
- Qualified according to JEDEC criteria

2. Applications

- Motor control and drive
- Battery management
- UPS (Uninterruptible Power Supplies)

3. Symbol



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering information

Part Number	Package	Brand
KND3203C	TO-252	KIA

5. Absolute maximum ratings

($T_A=25^\circ\text{C}$,unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-source voltage	V_{DS}	30	V
Continuous drain current	I_D	100	A
		80	A
		72	A
Pulse drain current ($T_C = 25^\circ\text{C}$, t_p limited by T_{jmax}) ¹	I_{DP}	320	A
Avalanche energy, single pulse	E_{AS}^2	248	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation ($T_C = 25^\circ\text{C}$)	P_D	92	W
Operating junction and storage temperature	T_J, T_{STG}	-55- 150	°C

6. Thermal characteristics

Parameter	Symbol	Max	Unit
Thermal resistance, Junction-ambient	$R_{\theta JA}$	105	°C/W
Thermal resistance, Junction-case	$R_{\theta JC}$	1.35	°C/W

7. Electrical characteristics

($T_A=25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{DS}}=250\mu\text{A}$	30	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.9	1.3	2.5	V
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}}=30\text{V}, V_{\text{GS}}=0\text{V}, T_J=25^\circ\text{C}$	-	-	1	μA
		$V_{\text{DS}}=24\text{V}, V_{\text{GS}}=0\text{V}, T_J=125^\circ\text{C}$	-	-	10	
Gate-source leakage current	I_{GSS}	$V_{\text{GS}}=20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	100	nA
Drain-source on-resistance ³	$R_{\text{DS(on)}}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=30\text{A}, T_J=25^\circ\text{C}$	-	3.2	4.0	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=15\text{A}$	-	4.7	8.0	
Forward transconductance	g_{fs}	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=15\text{A}$	-	20	-	S
Input capacitance	C_{iss}	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	-	3100	-	pF
Output capacitance	C_{oss}		-	340	-	
Reverse transfer capacitance	C_{rss}		-	300	-	
Turn-on delay time ^{3 4}	$t_{\text{d(on)}}$	$V_{\text{DD}}=15\text{V}, I_{\text{D}}=15\text{A}, R_{\text{G}}=3.3\Omega, V_{\text{GS}}=10\text{V}$	-	20	-	nS
Rise time ^{3 4}	t_{r}		-	44	-	
Turn-off delay time ^{3 4}	$t_{\text{d(off)}}$		-	53	-	
Fall time ^{3 4}	t_{f}		-	22	-	
Total gate charge ^{3 4}	Q_{g}	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}$	-	68	-	nC
Gate-source charge ^{3 4}	Q_{gs}		-	7.5	-	
Gate-drain charge ^{3 4}	Q_{gd}		-	21	-	
Gate resistance ^{3 4}	R_{g}	$V_{\text{DS}}=0\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	-	1.5	-	Ω
Body Diode forward voltage	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{SD}}=30\text{A}$	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$I_{\text{F}}=30\text{A}, \frac{di}{dt}=100\text{A}/\mu\text{s}$	-	25	-	nS
Body Diode Reverse Recovery charge	Q_{rr}		-	15	-	nC

Note :

- 1 .Repetitive Rating : Pulsed width limited by maximum junction temperature.
- 2 .The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=25\text{V}, V_{\text{GS}}=10\text{V}, L=0.5\text{mH}$.
3. The data tested by pulsed , pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$.
4. Essentially independent of operating temperature.

8. Test circuits and waveforms

Fig 1: Output Characteristics

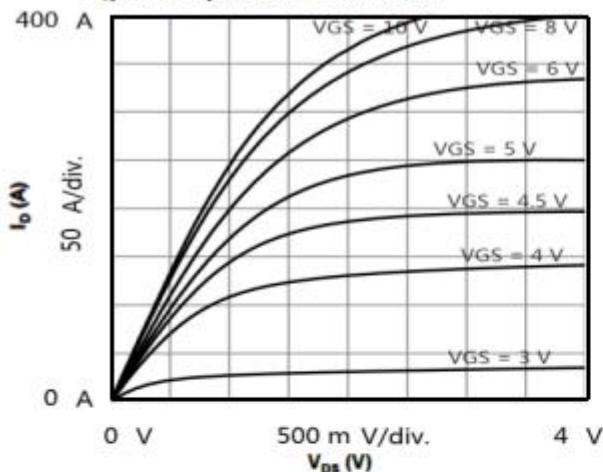


Fig 2: Transfer Characteristics

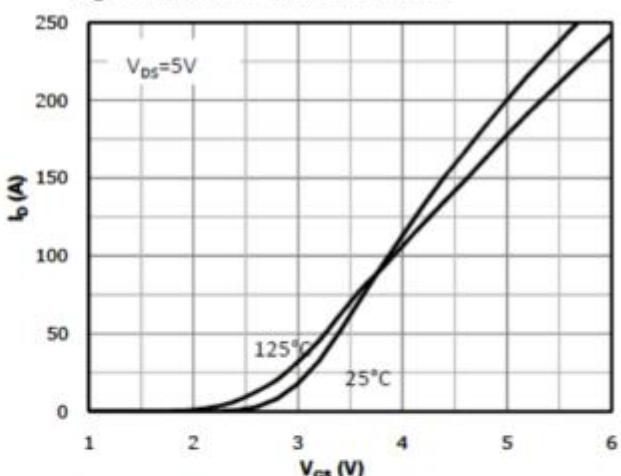


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

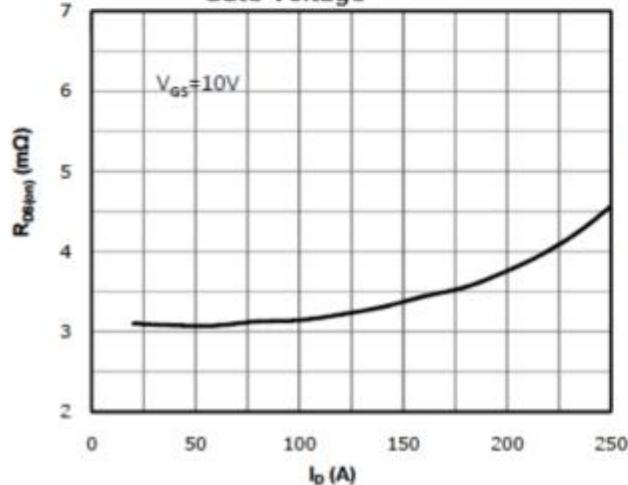


Fig 4: $R_{DS(on)}$ vs Gate Voltage

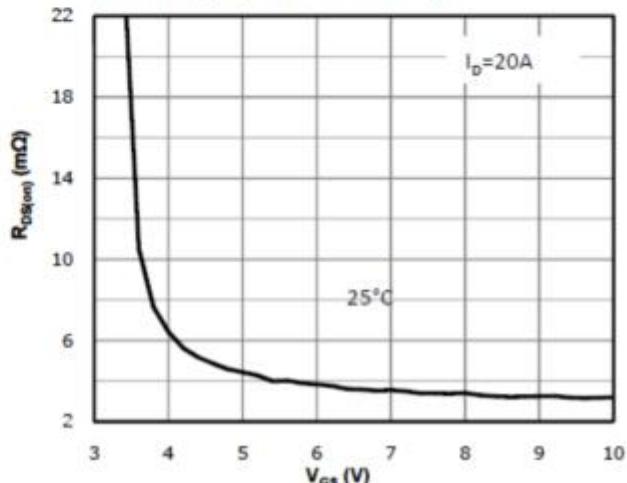


Fig 5: $R_{DS(on)}$ vs. Temperature

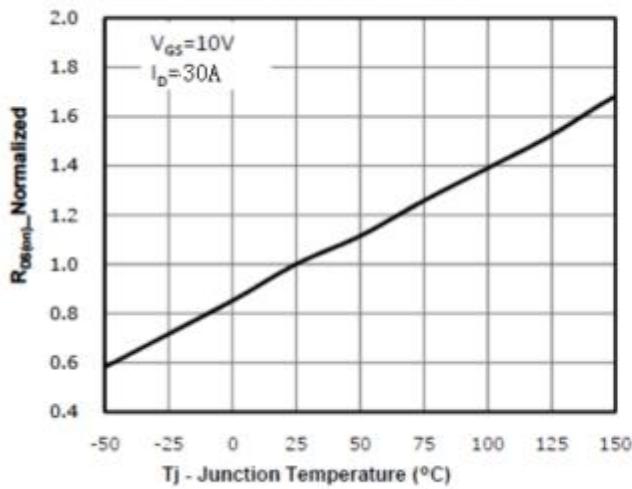


Fig 6: Capacitance Characteristics

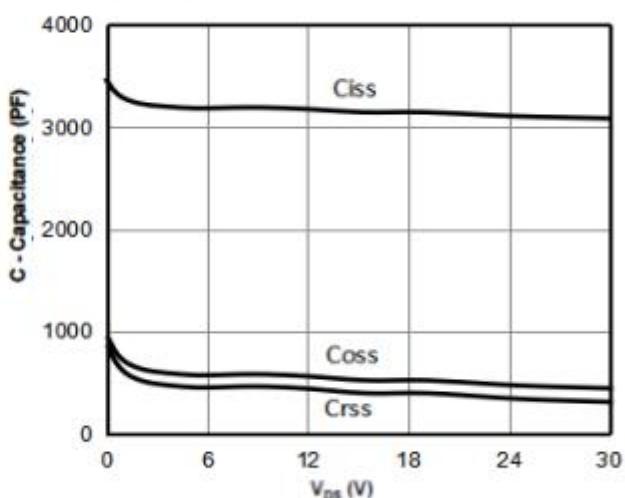


Fig 7: Gate Charge Characteristics

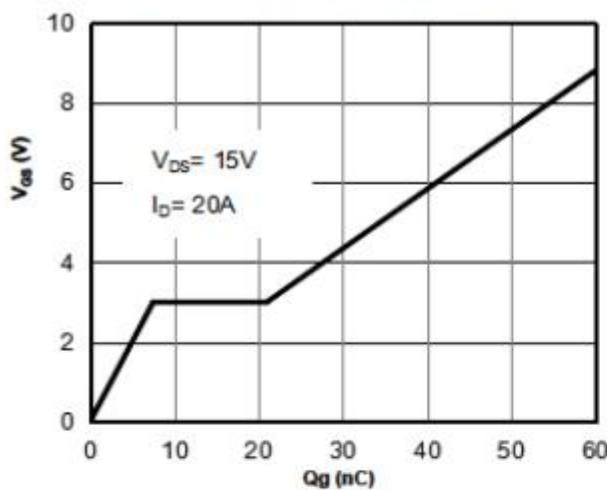


Fig 8: Body-diode Forward Characteristics

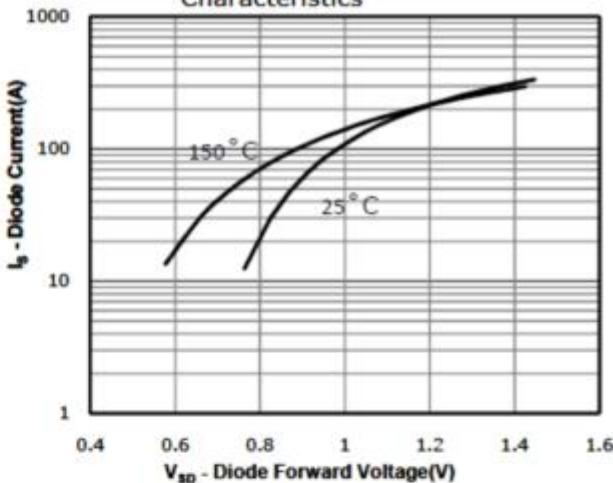


Fig 9: Power Dissipation

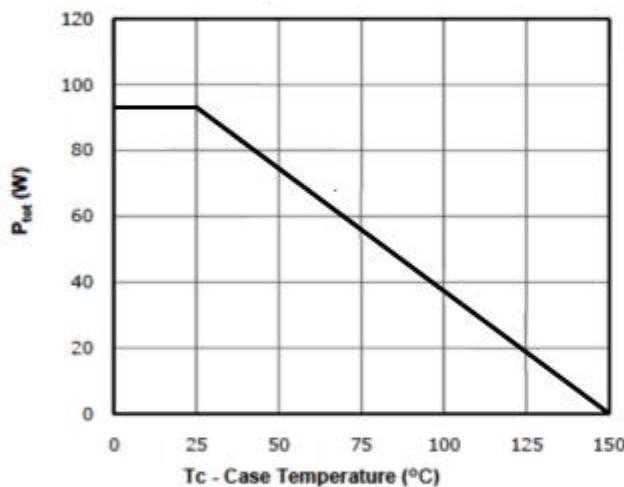


Fig 10: Drain Current Derating

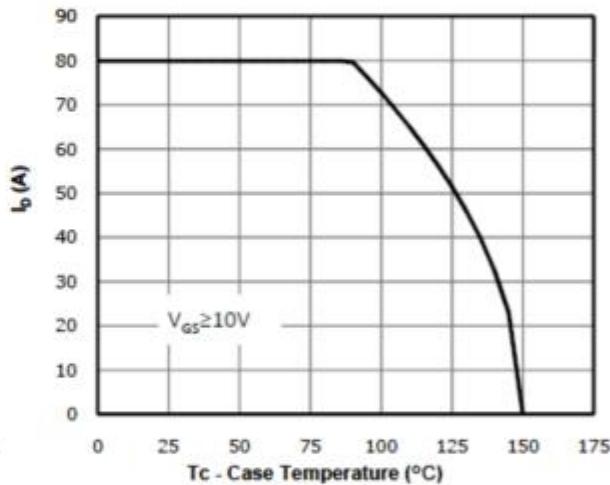


Fig 11: Safe Operating Area

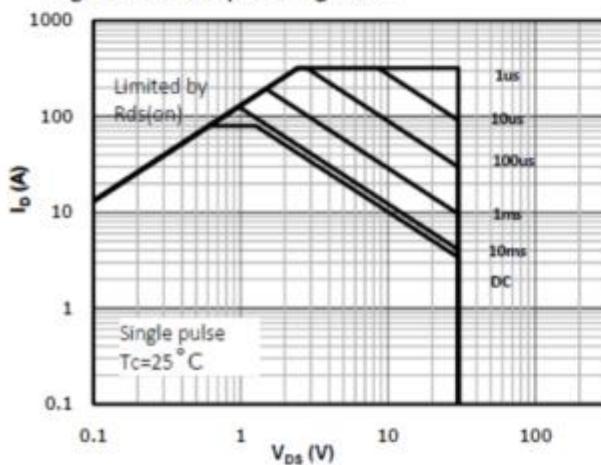


Fig 12: Max. Transient Thermal Impedance

