

## 1. Description

- SGT MOSFET technology
- Advanced Trench MOS Technology
- Low Gate Charge
- Low  $R_{DS(ON)}$
- 100% EAS Guaranteed
- Green Device Available

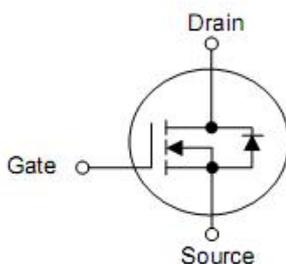
## 2. Features

- $R_{DS(ON)}=7.3m\Omega(\text{typ.}) @ V_{GS}=10V$

## 3. Applications

- Load Switch
- LED Applications
- Networking Applications
- Quick Charger

## 4. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source

## 5. Ordering Information

Part Number	Package	Brand
KCP2915B	TO-220	KIA

## 6. Absolute maximum ratings

TC=25°C unless otherwise specified

Parameter	Symbol	Ratings	Unit	
Drain-to-Source Voltage	$V_{DS}$	150	V	
Gate-to-Source Voltage	$V_{GS}$	±20	V	
Continuous Drain Current <sup>1)</sup>	$T_C=25^\circ\text{C}$	$I_D$	130	A
	$T_C=100^\circ\text{C}$	$I_D$	80	A
Pulsed Drain Current <sup>2)</sup>	$I_{DM}$	450	A	
Avalanche Energy <sup>3)</sup>	EAS	784	mJ	
Avalanche Current	$I_{AS}$	56	A	
Total Power Dissipation <sup>4)</sup>	$P_D$	178	W	
Operation Junction Temperature Range	$T_J$	-55 to 150	°C	
Storage Temperature Range	$T_{STG}$	-55 to 150	°C	

## 7. Thermal characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient <sup>1)</sup>	$R_{\theta JA}$	-	50	°C/W
Thermal Resistance, Junction-to-Case <sup>1)</sup>	$R_{\theta JC}$	-	0.7	°C/W

## 8. Electrical characteristics

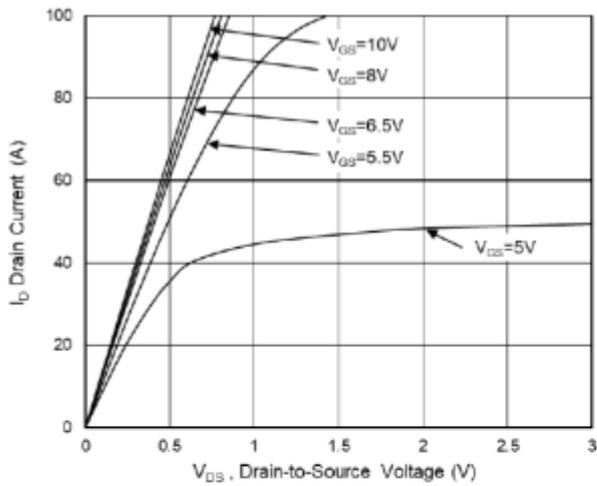
 (T<sub>J</sub>=25°C, unless otherwise notes)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	150	-	-	V
Static Drain-Source On-Resistance <sup>2)</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	7.3	9	mΩ
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	2	3	4	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =120V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	-	-	1	uA
		V <sub>DS</sub> =120V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	-	-	5	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Resistance	R <sub>g</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	-	1.9	-	Ω
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =75V, V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	110	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	25.9	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	31.8	-	nC
Turn-On Delay Time	T <sub>d(on)</sub>	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =1A	-	33	-	ns
Rise Time	T <sub>r</sub>		-	26	-	ns
Turn-Off Delay Time	T <sub>d(off)</sub>		-	98	-	ns
Fall Time	T <sub>f</sub>		-	90	-	ns
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =75V, V <sub>GS</sub> =0V, f=1MHz	-	5750	-	pF
Output Capacitance	C <sub>oss</sub>		-	414	-	pF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	9.5	-	pF
Continuous Source Current <sup>1)</sup>	I <sub>S</sub>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	-	-	130	A
Diode Forward Voltage <sup>2)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	-	-	1.2	V

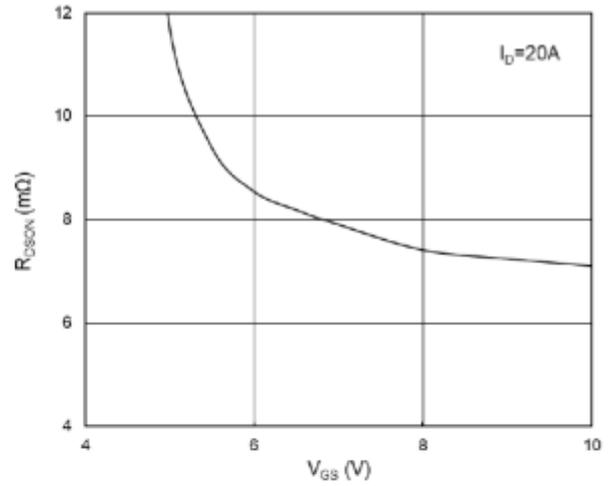
Notes:

- 1) The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2) The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3) The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=50V, V<sub>GS</sub>=10V, L=0.5mH, I<sub>AS</sub>=56A
- 4) The power dissipation is limited by 150°C junction temperature.
- 5) The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

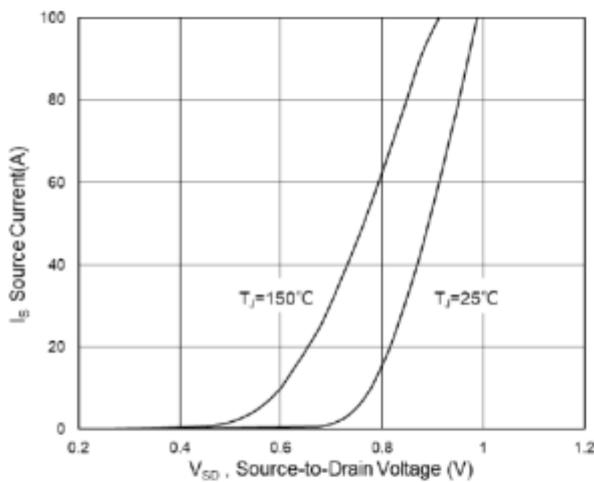
**9. Typical Characteristics**



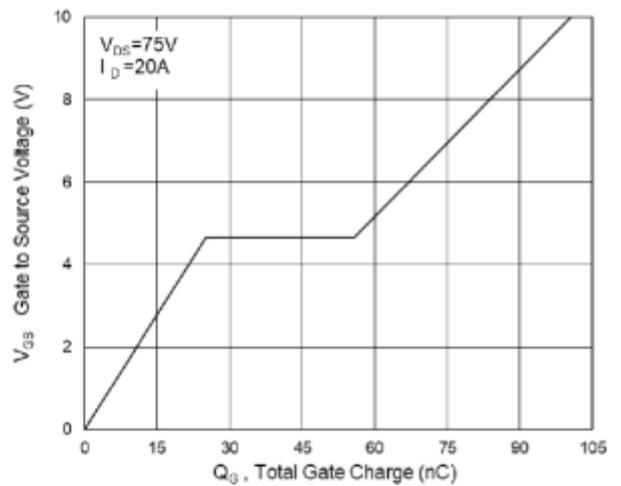
**Fig.1 Typical Output Characteristics**



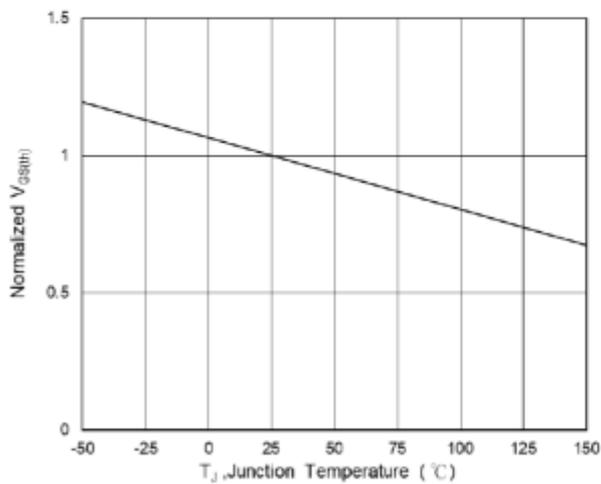
**Fig.2 On-Resistance vs G-S Voltage**



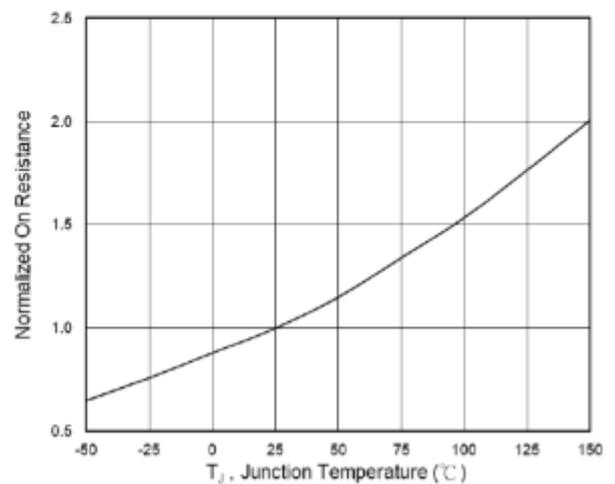
**Fig.3 Source Drain Forward Characteristics**



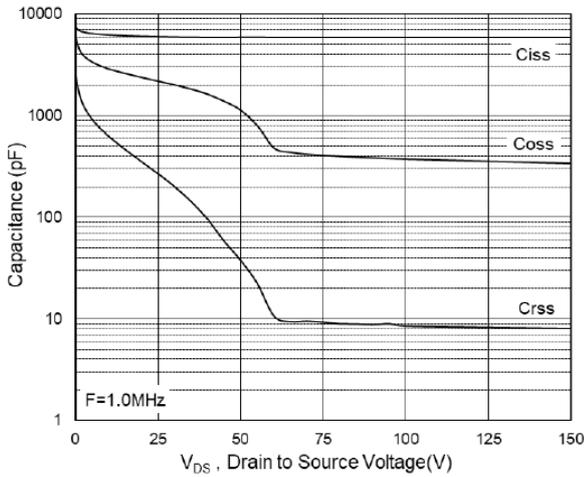
**Fig.4 Gate-Charge Characteristics**



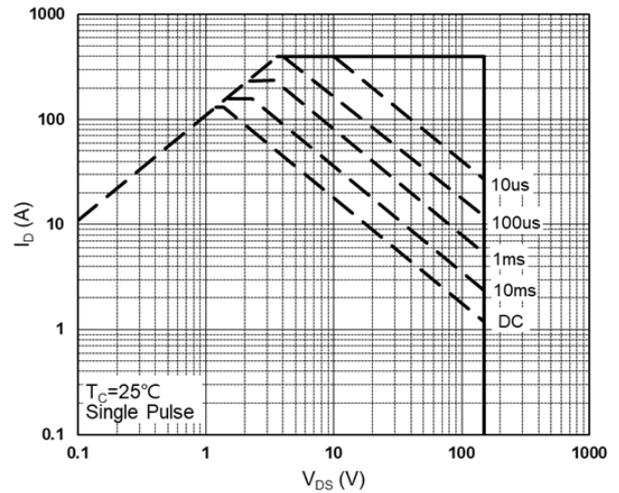
**Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$**



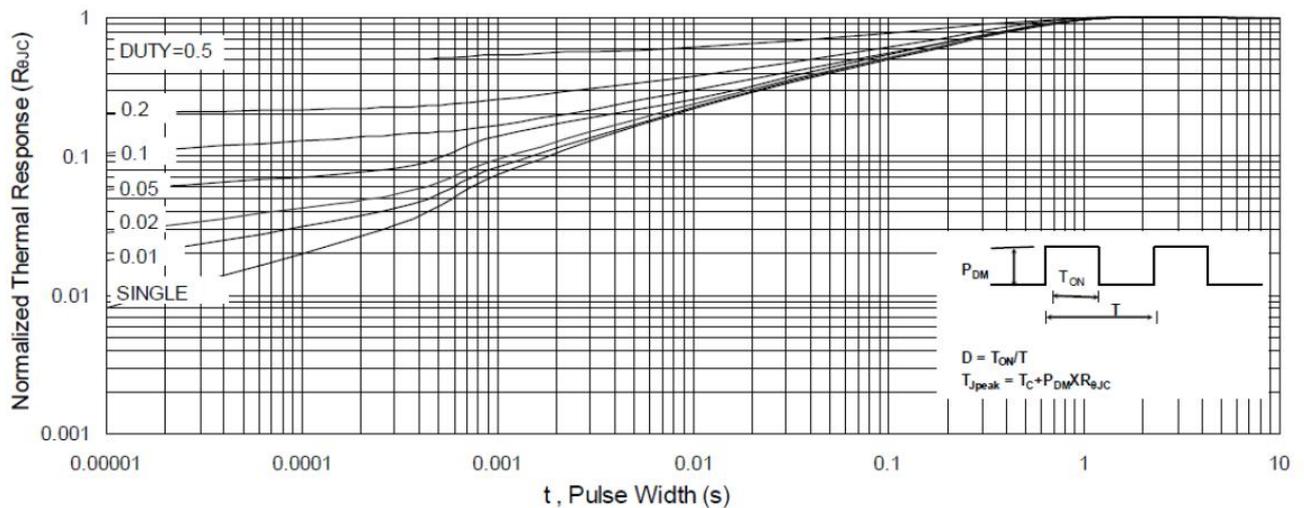
**Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$**



**Fig.7 Capacitance**

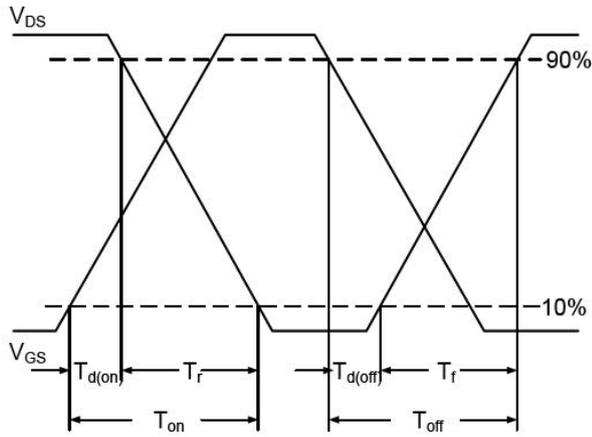


**Fig.8 Safe Operating Area**

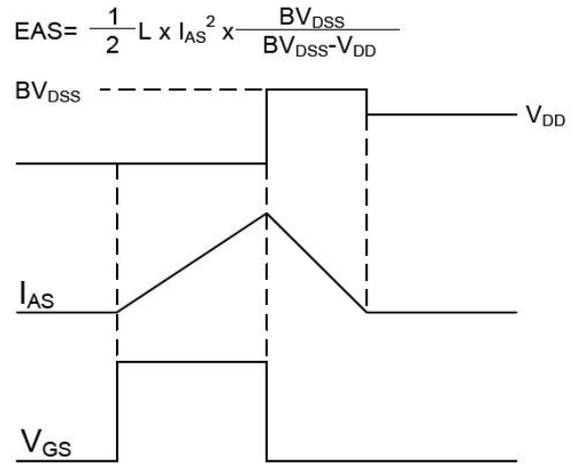


**Fig.9 Normalized Maximum Transient Thermal Impedance**

**10. Test Circuits and Waveforms**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**