

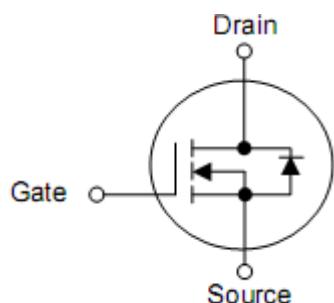
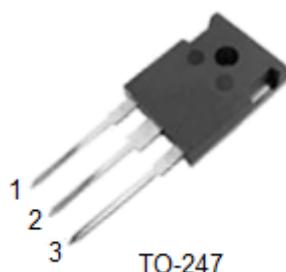
## 1. Features

- RoHS Compliant
- $R_{DS(ON)}=1.0\Omega(\text{typ.}) @ V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

## 2. Applications

- Adaptor
- Charger
- SMPS Standby Power

## 3. Symbol



Pin	Function
1	Gate
2	Drain
3	Source

## 4. Ordering Information

Part Number	Package	Brand
KNM61100A	TO-247	KIA

## 5. Absolute maximum ratings

$T_C=25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Rating	Units
Drain-source voltage <sup>1)</sup>	$V_{DSS}$	1000	V
Gate-to-Source Voltage	$V_{GSS}$	$\pm 30$	V
Continuous drain current	$I_D$	10	A
Pulsed Drain Current at $V_{GS}=10\text{V}$	$I_{DM}$	40	A
Single pulse avalanche energy	$E_{AS}$	900	mJ
Power dissipation	$P_D$	298	W
Derating factor above $25^\circ\text{C}$		2.38	W/ $^\circ\text{C}$
Soldering Temperature Distance of 1.6mm from case for 10 seconds	$T_L$	300	$^\circ\text{C}$
Operating junction and storage temperature range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

## 6. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance junction-case	$R_{\theta JC}$	0.42	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	55	$^\circ\text{C/W}$

## 7. Electrical characteristics

( $T_J=25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	1000	-	-	V
Drain-source leakage current	$I_{\text{DSS}}$	$V_{\text{DS}}=1000\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{\text{DS}}=800\text{V}, V_{\text{GS}}=0\text{V}, T_C=125^\circ\text{C}$	-	-	100	
Gate-source forward leakage	$I_{\text{GSS}}$	$V_{\text{GS}}=\pm30\text{V}, V_{\text{DS}}=0\text{V}$	-	-	$\pm100$	nA
Drain-source on-resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=5\text{A}$	-	1.0	1.25	$\Omega$
Gate threshold voltage	$V_{\text{GS(TH)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	2.5	-	4.5	V
Forward transconductance	$g_{\text{fs}}$	$V_{\text{DS}}=15\text{V}, I_{\text{D}}=5\text{A}$	-	7.0	-	S
Input capacitance	$C_{\text{iss}}$	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}$ $f=1\text{MHz}$	-	2800	-	pF
Reverse transfer capacitance	$C_{\text{rss}}$		-	46	-	pF
Output capacitance	$C_{\text{oss}}$		-	248	-	pF
Total gate charge	$Q_g$	$V_{\text{DD}}=500\text{V}, I_{\text{D}}=10\text{A}$ $V_{\text{GS}}=0\sim10\text{V}$	-	71	-	nC
Gate-source charge	$Q_{\text{gs}}$		-	15	-	nC
Gate-drain charge	$Q_{\text{gd}}$		-	30	-	nC
Turn-on delay time	$t_{\text{d(on)}}$	$V_{\text{DD}}=500\text{V}, V_{\text{GS}}=10\text{V}, R_{\text{G}}=9.1\Omega, I_{\text{D}}=10\text{A}$	-	46	-	ns
Rise time	$t_r$		-	49	-	ns
Turn-off delay time	$t_{\text{d(off)}}$		-	58	-	ns
Fall time	$t_f$		-	54	-	ns
Continuous Source Current <sup>2)</sup>	$I_{\text{SD}}$	Integral pn-diode in MOSFET	-	-	10	A
Pulsed Source Current <sup>2)</sup>	$I_{\text{SM}}$		-	-	40	
Diode forward voltage	$V_{\text{SD}}$	$I_{\text{S}}=10\text{A}, V_{\text{GS}}=0\text{V},$	-	-	1.5	V
Reverse Recovery Time	$t_{\text{rr}}$	$V_{\text{GS}}=0\text{V}, I_{\text{F}}=10\text{A}, \frac{dI_{\text{F}}}{dt}=100\text{A}/\mu\text{s}$	-	850	-	nS
Reverse Recovery Charge	$Q_{\text{rr}}$		-	4.4	-	$\mu\text{C}$

Note:

1)  $T_J=+25^\circ\text{C}$  to  $+150^\circ\text{C}$ .

2) Pulse width  $\leq 380\text{us}$ ; duty cycle  $\leq 2\%$ .

## 8. Typical operating characteristics

Fig. 1 Output Characteristics

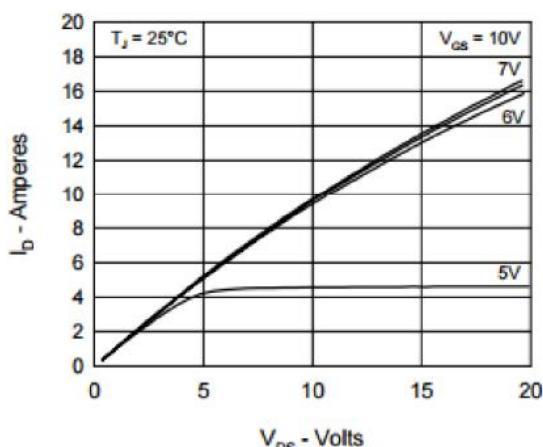


Fig. 2 Input Admittance

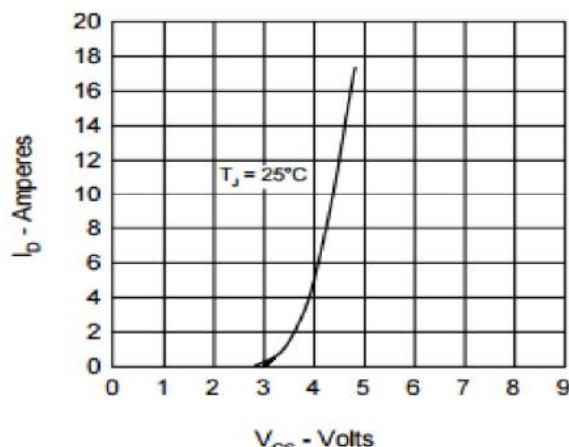


Fig. 3  $R_{DS(on)}$  vs. Drain Current

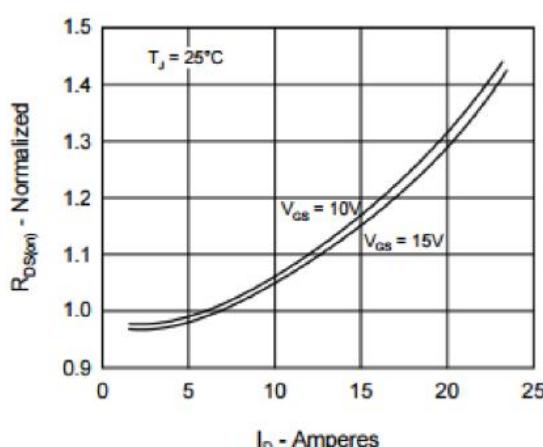


Fig. 5 Drain Current vs. Case Temperature

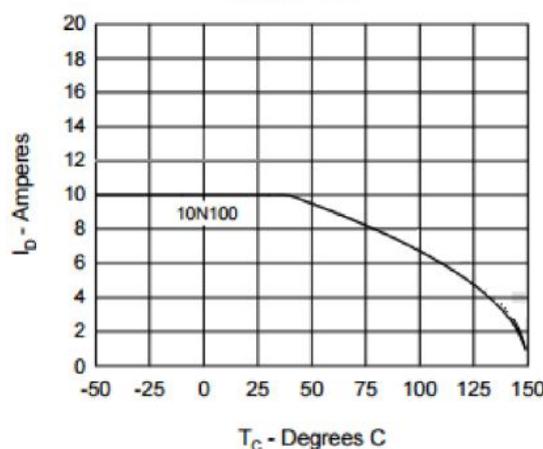


Fig. 4 Temperature Dependence of Drain to Source Resistance

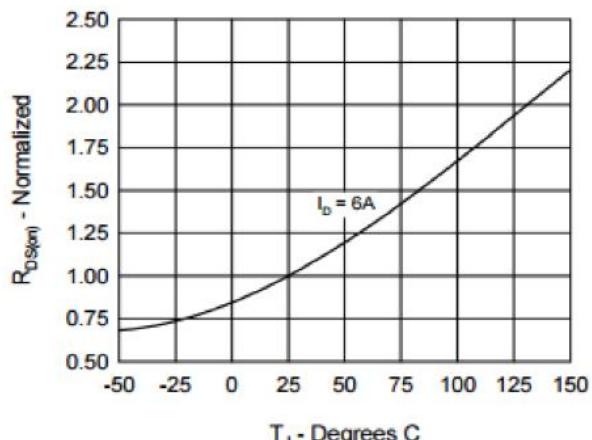


Fig. 6 Temperature Dependence of Breakdown and Threshold Voltage

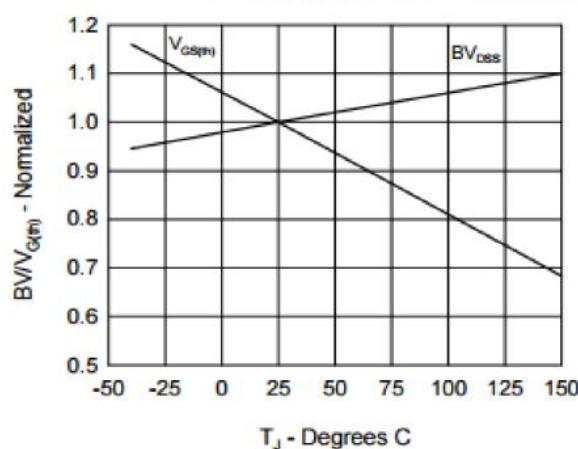


Fig.7 Gate Charge Characteristic Curve

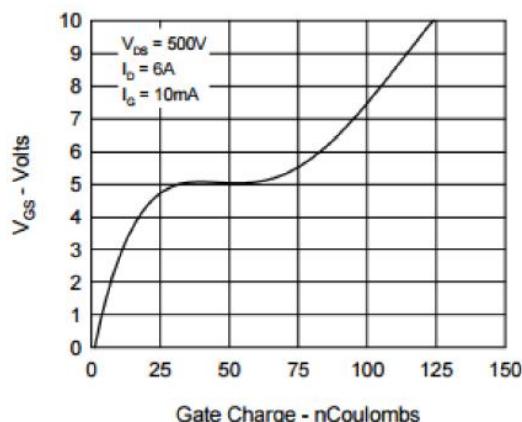


Fig.9 Capacitance Curves

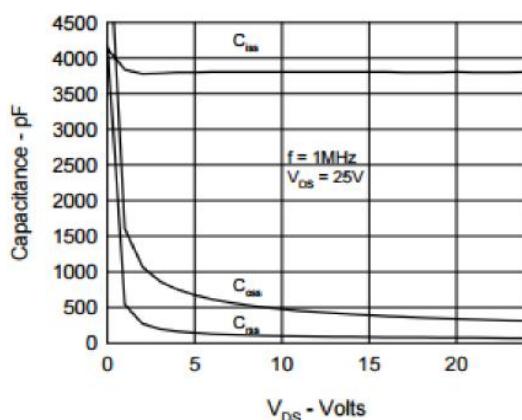


Fig.11 Transient Thermal Impedance

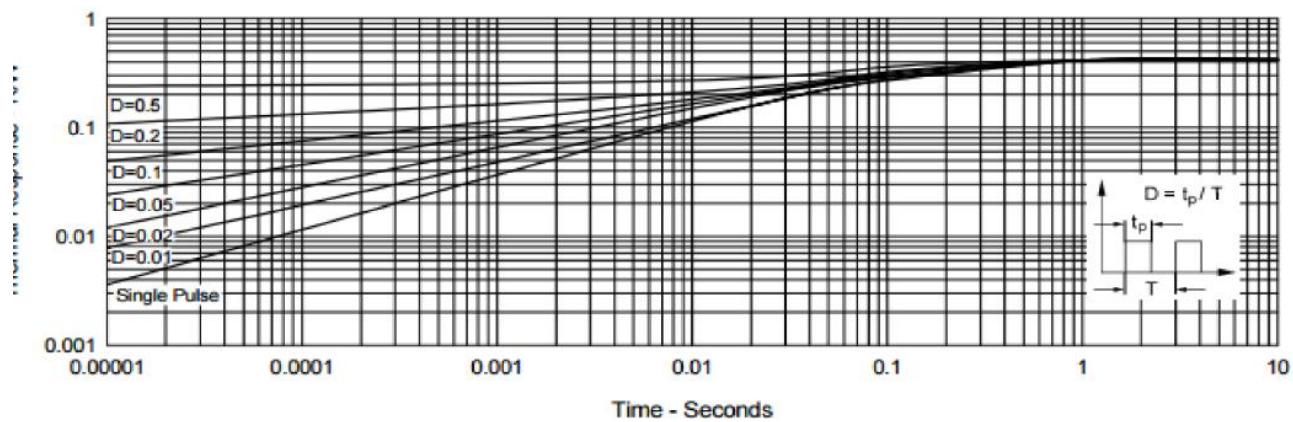


Fig.8 Forward Bias Safe Operating Area

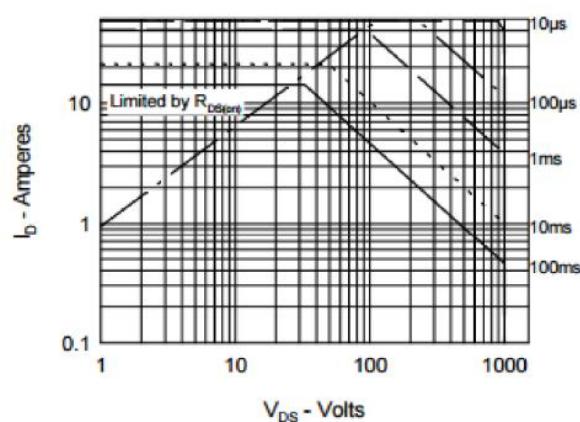
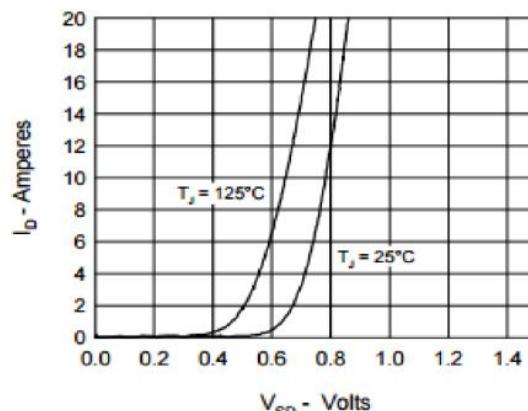


Fig.10 Source Current vs. Source to Drain Voltage



## 9. Test Circuits and Waveform

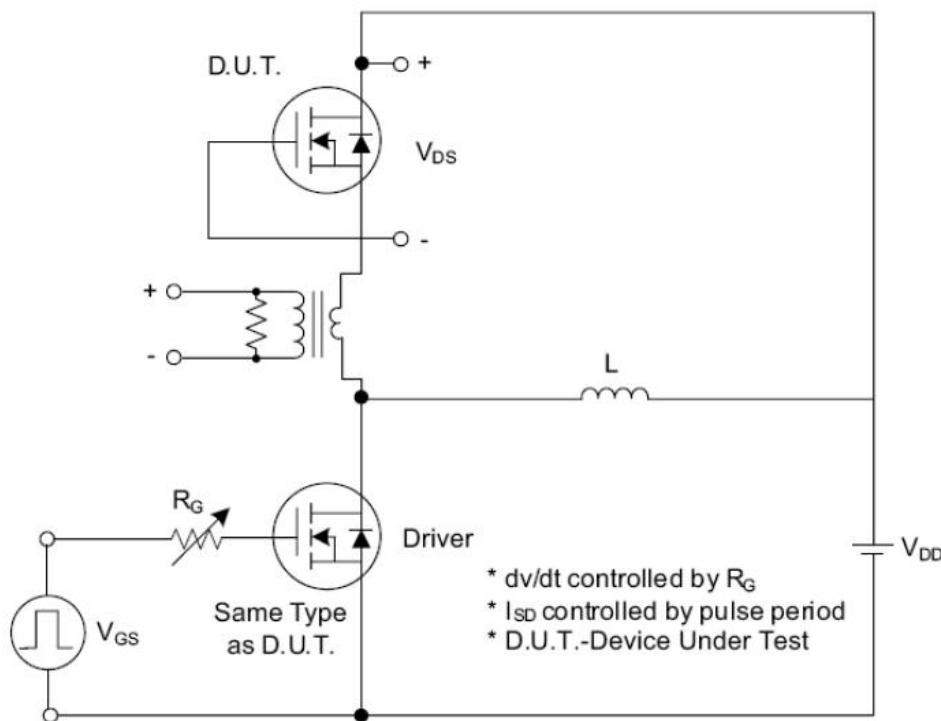


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

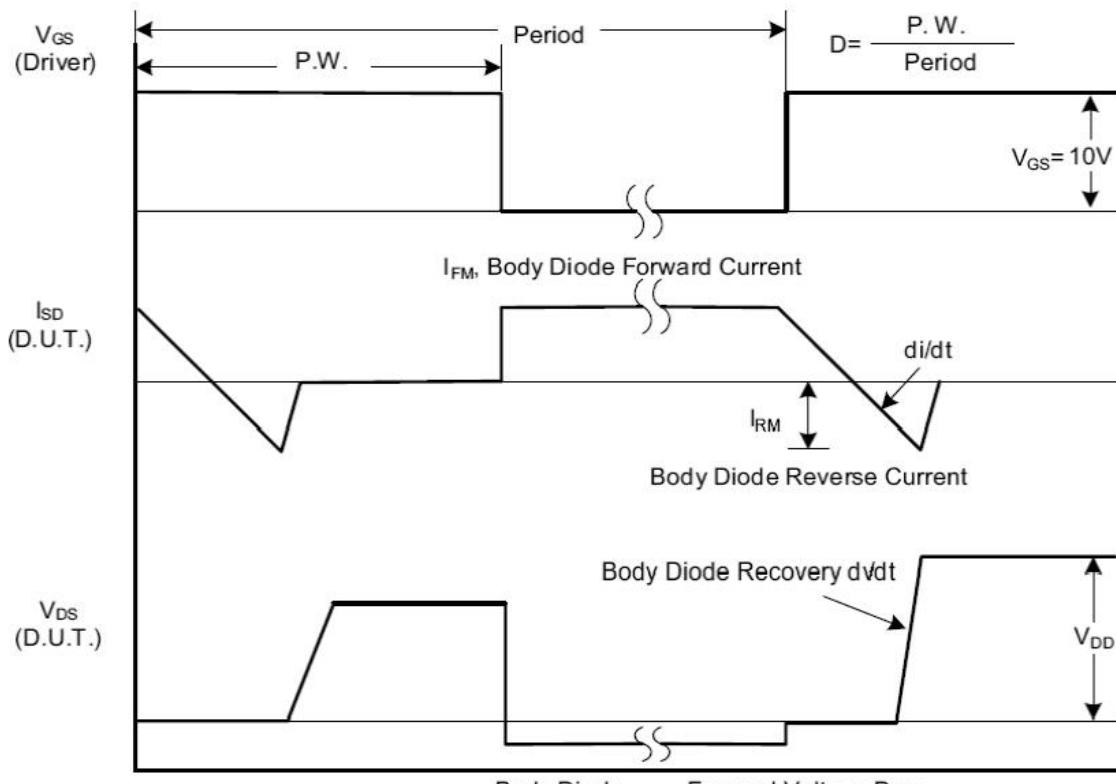


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

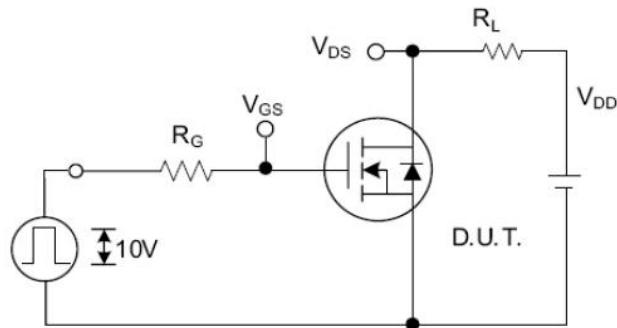


Fig. 2.1 Switching Test Circuit

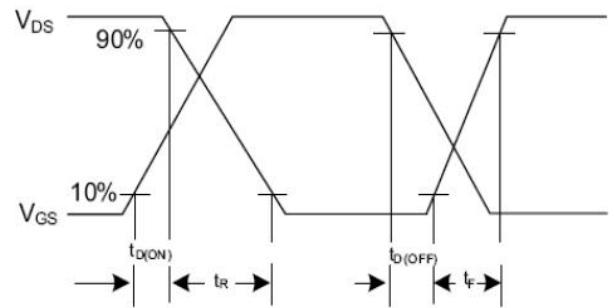


Fig. 2.2 Switching Waveforms

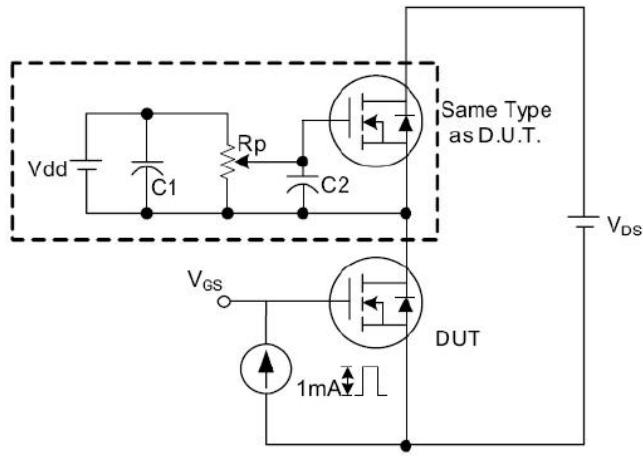


Fig. 3 . 1 Gate Charge Test Circuit

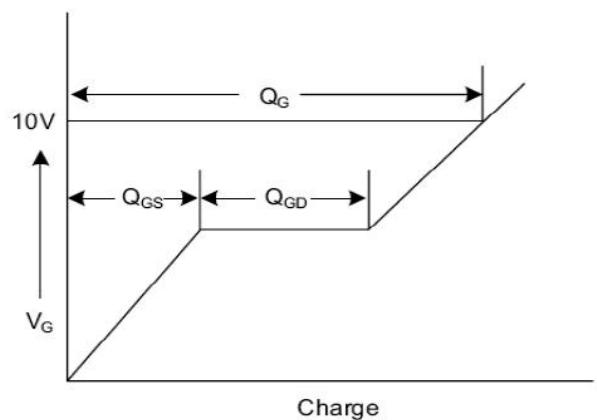


Fig. 3 . 2 Gate Charge Waveform

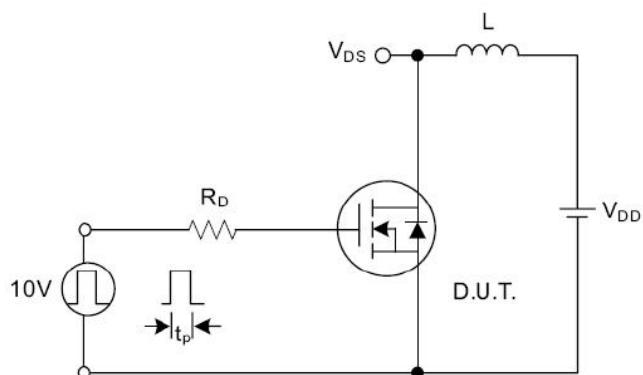


Fig. 4.1 Unclamped Inductive Switching Test Circuit

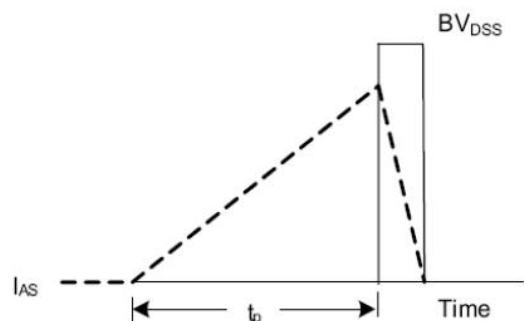


Fig. 4.2 Unclamped Inductive Switching Waveforms